

Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1)-6) (cancelled)

7) (previously presented) A phase locked loop circuit, comprising:

- a phase-frequency detector to provide a phase difference signal in response to an input signal and a feedback signal;

- a first charge-pump, coupled to the phase-frequency detector, to provide a first voltage in response to the phase difference signal;

- a second charge-pump, coupled to the phase-frequency detector, to provide a second voltage in response to the phase difference signal;

- a loop resistor, coupled to the first charge-pump, to provide a buffered voltage responsive to the first voltage;

- a voltage regulator, coupled to the loop resistor and the second charge-pump, to provide a current in response to the buffered voltage and second voltage, wherein the voltage regulator includes a bias-generating device to provide a bias current;

- a voltage-controlled oscillator, coupled to the voltage regulator, to provide the feedback signal in response to the current; and,

- an interconnect, coupled to the voltage regulator, the first charge-pump, and the second charge-pump, to transfer the bias current,

- wherein the bias-generating device in the voltage regulator is a MOSFET device,

- wherein the MOSFET device is a first p-type transistor having a drain coupled to the interconnect and the first p-type transistor having a source coupled a voltage source,

- wherein the voltage regulator includes:

- a second p-type transistor having a gate coupled to a gate of the first p-type transistor and the second p-type transistor having a source coupled to the voltage source;

- a third p-type transistor having a gate coupled to the gate of the second p-type transistor and the third p-type transistor having a source coupled to the voltage source;

- a fourth p-type transistor having a gate coupled to the gate of the third p-type transistor and the fourth p-type transistor having a source coupled to the voltage source;

- a fifth p-type transistor having a gate coupled to the gate of the fourth p-type transistor and the fifth p-type transistor having a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, the first n-type transistor having a source coupled to ground and the first n-type transistor having a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain of the third p-type transistor, the drain of the second n-type transistor coupled to the gate of the third p-type transistor and the gate of the fourth p-type transistor, the second n-type transistor having a gate coupled to an input, and the second n-type transistor having a source;

a third n-type transistor having a drain coupled to a drain of the fourth p-type transistor and a drain of the fifth p-type transistor, the third n-type transistor having a gate coupled to an output and the gate of the third n-type transistor coupled to the drain of the fourth p-type transistor and the drain of the fifth p-type transistor, and the third n-type transistor having a source; and,

a fourth n-type transistor having a drain coupled to the source of the second n-type transistor and the source of the third n-type transistor, the fourth n-type transistor having a source coupled to ground and the fourth n-type transistor having a gate coupled to the gate of the first n-type transistor and the drain of the first n-type transistor.

8)-10) (cancelled)

11) (previously presented) A delay locked loop circuit, comprising:

a phase detector to generate a phase difference signal in response to an input signal and a feedback signal;

a charge-pump, coupled to the phase detector, to generate a voltage in response to the phase difference signal;

a voltage regulator, coupled to the charge-pump, to provide a current in response to the voltage, wherein the voltage regulator includes a bias-generating device to provide a bias current;

a voltage-controlled delay line, coupled to the voltage regulator, to provide the feedback signal in response to the current; and,

an interconnect, coupled to the charge-pump and the voltage regulator, to transfer the bias current,

wherein the bias-generating device in the voltage regulator is a MOSFET device,

wherein the MOSFET device is a first p-type transistor having a drain coupled to the interconnect and the first p-type transistor having a source coupled to a voltage source,

wherein the voltage regulator includes:

a second p-type transistor having a gate coupled to a gate of the first p-type transistor and the second p-type transistor having a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the gate of the second p-type transistor and the third p-type transistor having a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the gate of the third p-type transistor and the fourth p-type transistor having a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the gate of the fourth p-type transistor and the fifth p-type transistor having a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, the first n-type transistor having a source coupled to ground and the first n-type transistor having a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain of the third p-type transistor, the drain of the second n-type transistor coupled to the gate of the third p-type transistor and the gate of the fourth p-type transistor, the second n-type transistor having a gate coupled to an input, and the second n-type transistor having a source;

a third n-type transistor having a drain coupled to a drain of the fourth p-type transistor and a drain of the fifth p-type transistor, the third n-type transistor having a gate coupled to an output and the gate of the third n-type transistor coupled to the drain of the fourth p-type transistor and the drain of the fifth p-type transistor, and the third n-type transistor having a source; and,

a fourth n-type transistor having a drain coupled to the source of the second n-type transistor and the source of the third n-type transistor, the fourth n-type transistor having a source coupled to ground and the fourth n-type transistor having a gate coupled to the gate of the first n-type transistor and the drain of the first n-type transistor.

12)-23)(cancelled)

24) (previously presented) A circuit, comprising:

a first p-type transistor having a gate, the first p-type transistor having a drain to

output a current proportional to an output current and the first p-type transistor having a source coupled to a voltage source;

a second p-type transistor having a gate coupled to the gate of the first p-type transistor and the second p-type transistor having a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the gate of the second p-type transistor and the third p-type transistor having a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the gate of the third p-type transistor and the fourth p-type transistor having a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the gate of the fourth p-type transistor and the fifth p-type transistor having a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, the first n-type transistor having a source coupled to ground and the first n-type transistor having a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain of the third p-type transistor, the drain of the second n-type transistor coupled to the gate of the third p-type transistor and the gate of the fourth p-type transistor, the second n-type transistor having a gate coupled to an input, and the second n-type transistor having a source;

a third n-type transistor having a drain coupled to a drain of the fourth p-type transistor and a drain of the fifth p-type transistor, the third n-type transistor having a gate coupled to an output and the gate of the third n-type transistor coupled to the drain of the fourth p-type transistor and the drain of the fifth p-type transistor, and the third n-type transistor having a source; and,

a fourth n-type transistor having a drain coupled to the source of the second n-type transistor and the source of the third n-type transistor, the fourth n-type transistor having a source coupled to ground and the fourth n-type transistor having a gate coupled to a gate of the first n-type transistor.

- 25) (previously presented) The circuit of claim 24, wherein the circuit is included in an operational amplifier to generate a buffered signal at the output in response to a signal at the input.

26)-37)(cancelled)

- 38) (original) A phase locked loop circuit, comprising:
a phase-frequency detector;
a charge-pump;
a voltage regulator to output a regulated voltage and a load current; and
a voltage-controlled oscillator to input the regulated voltage and the load current, the
voltage-controlled oscillator to output a signal having a frequency based on the regulated
voltage,
wherein the voltage regulator provides a first bias current to the charge-pump based
on the load current.
- 39) (currently amended) The phase locked loop circuit of claim 38, wherein the charge-pump
includes a semiconductor device to ~~output~~ provide the first bias current in response to the
load current.
- 40) (original) The phase locked loop circuit of claim 38, further comprising:
a loop resistor,
wherein the voltage regulator provides a second bias current to the loop resistor
based on the load current.
- 41) (original) The phase locked loop circuit of claim 40, further comprising:
another charge-pump,
wherein the voltage regulator provides a third bias current to the another charge-
pump based on the load current.
- 42) (original) The phase locked loop circuit of claim 41, further comprising:
a phase mixer,
wherein the voltage regulator provides a fourth bias current to the phase mixer based
on the load current.
- 43) (original) The phase locked loop circuit of claim 42, further comprising:
a clock buffer,

wherein the voltage regulator provides a fifth bias current to the clock buffer based on the load current.

- 44) (original) A delay locked loop circuit, comprising:
a phase detector;
a charge-pump;
a voltage regulator to output a regulated voltage and a load current; and
a voltage-controlled delay line to input the regulated voltage and the load current, the voltage-controlled delay line to output a signal having a frequency based on the regulated voltage,
wherein the voltage regulator provides a first bias current to the charge-pump based on the load current.
- 45) (currently amended) The delay locked loop circuit of claim 44, wherein the charge-pump includes a semiconductor device to ~~output~~ provide the first bias current in response to the load current.
- 46) (original) The delay locked loop circuit of claim 44, further comprising:
a phase mixer,
wherein the voltage regulator provides a second bias current to the phase mixer based on the load current.
- 47) (original) The delay locked loop circuit of claim 46, further comprising:
a clock buffer,
wherein the voltage regulator provides a third bias current to the clock buffer based on the load current.